AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Original) A bonding pad structure, comprising:

a substrate having a bonding region and a sensing region;

a first dielectric layer formed overlying the substrate and having a dielectric island surrounded by a ring-shaped trench;

a first conductive layer formed in the ring-shaped trench of the first dielectric layer;

a passivation layer formed overlying the first dielectric layer and having an opening, wherein the opening corresponds to the bonding region and the sensing region and exposes the dielectric island and a part of the first conductive layer; and

a second conductive layer covering the opening of the passivation layer and electrically connected to the first conductive layer.

2. (Original) The bonding pad structure as claimed in claim 1, wherein the substrate further comprises:

a main area comprising an active area and a peripheral area;

a first scribe line extending along a first direction; and

a second scribe line extending along a second direction, wherein the intersection of the first scribe line and the second scribe line defines the main area;

wherein, the bonding pad structure is formed overlying the active area, the peripheral area, the first scribe line, the second scribe line or a combination thereof.

3. (currently amended): A chip comprising bonding pad structures ~~The bonding pad structure~~ as claimed in claim 2, wherein the bonding pad structures are arranged in a single line or staggered.

4. (Original) The bonding pad structure as claimed in claim 1, wherein the width of the first conductive layer is 1~50μm.

5. (Original) The bonding pad structure as claimed in claim 1, wherein the depth of the first conductive layer is 0.5~2μm.

6. (Original) The bonding pad structure as claimed in claim 1, wherein a measurement ratio R_1 satisfies the formula: $R_1 = A_r/A_s$ and $0 \leq R_1 \leq 30\%$, where A_r is an area of the first conductive layer within the sensing region, and A_s is the area of the sensing region.

7. (Original) The bonding pad structure as claimed in claim 1, further comprising:

a second dielectric layer formed underlying the first dielectric layer;

a third conductive layer formed in the second dielectric layer; and

at least one conductive plug formed in the second dielectric layer and electrically connecting the third conductive layer to the first conductive layer.

8. (Original) The bonding pad structure as claimed in claim 7, wherein the third conductive layer is a ring, a lattice form, an array of islands or a solid form.

9. (Original) The bonding pad structure as claimed in claim 1, wherein the trench of the first dielectric layer is a quadrilateral ring, a circular ring, a hexagonal ring, an octagonal ring or a polygonal ring.

10. (Original) The bonding pad structure as claimed in claim 1, wherein the first conductive layer is a quadrilateral ring, a circular ring, a hexagonal ring, an octagonal ring or a polygonal ring.

11. (Original) The bonding pad structure as claimed in claim 1, wherein the second conductive layer is a quadrilateral solid, a circular solid, a hexagonal solid, an octagonal solid or a polygonal solid.

12. (Original) The bonding pad structure as claimed in claim 1, further comprising at least one corner cut portion adjacent to at least one corner of the first conductive layer, wherein the corner cut portion prohibits the formation of the first conductive layer and allows the formation of the first dielectric layer.

13. (Original) The bonding pad structure as claimed in claim 12, wherein the corner cut portion is a right triangle, the hypotenuse length of the right triangle is 0.5~5μm, and an included angle θ_1 between the hypotenuse and X axis is 10°~80°.

14. (Currently amended) The bonding pad structure as claimed in claim 12, wherein a measurement ratio R_2 satisfies the formula: $R_2 = A_{t1}/A_{c1}$, $A_{c1} = W_1 \times W_2$, and $0 < R_2 < 80\%$, where A_{t1} is the area of the corner cut portion, A_{c1} is the corner area of the first conductive layer, W_1 is a first-direction width of the corner area of the first conductive layer, and W2 is a second-direction width of the corner area of the first conductive layer.

15. (Original) The bonding pad structure as claimed in claim 1, further comprising at least one corner cut portion adjacent to at least one corner of the second conductive layer, wherein the corner cut portion prohibits the formation of the second conductive layer and allows the formation of the passivation layer.

16. (Currently amended) The bonding pad structure as claimed in claim 15, wherein the corner cut portion is a right triangle, the hypotenuse length of the right triangle is 0.5~10μm, and an included angle θ[1]2 between the hypotenuse and X axis is 10°~80°.

17. (Original) The bonding pad structure as claimed in claim 1, wherein the first conductive layer further comprises at least one marking notch which delineates the sensing region from the bonding region.

18. (Original) The bonding pad structure as claimed in claim 17, wherein the marking notch of the first conductive layer comprises a bottom side and two lateral sides which surround the first dielectric layer to define a dielectric marking.

19. (Original) The bonding pad structure as claimed in claim 18, wherein a first length of the dielectric marking parallel to the bottom side of the marking notch is 1~3μm, and a second length of the dielectric marking parallel to the lateral side of the marking notch is 0.5~2μm.

20. (Original) The bonding pad structure as claimed in claim 1, wherein the second conductive layer further comprises at least one marking notch which delineates the sensing region from the bonding region.

21. (Original) The bonding pad structure as claimed in claim 20, wherein the marking notch of the second conductive layer comprises a bottom side and two lateral sides which surround the passivation dielectric layer to define a passivation marking.

22. (Original) The bonding pad structure as claimed in claim 21, wherein a first length of the passivation marking parallel to the bottom side of the marking notch is 1~3μm, and a second length of the passivation marking parallel to the lateral side of the marking notch is 0.5~2μm.

23. (Original) The bonding pad structure as claimed in claim 1, further comprising:

an extension portion of the first conductive layer extending away from the bonding region and the sensing region; and

a circuit under pad (CUP) scheme formed underlying the extension portion of the first conductive layer.

24. (Original) The bonding pad structure as claimed in claim 23, wherein the circuit under pad (CUP) scheme comprises:

a circuit scheme formed underlying the extension portion of the first conductive layer; and

a plurality of conductive plugs electrically connecting the circuit scheme to the extension portion of the first conductive layer.

25. (Original) The bonding pad structure as claimed in claim 24, wherein the circuit under pad (CUP) scheme comprises:

a buffer layer formed underlying the first dielectric layer, wherein the circuit scheme is formed in the buffer layer; and

a plurality of via holes formed in the first dielectric layer and underlying the extension portion of the first conductive layer, wherein the conductive plugs are formed in the via holes respectively.

26. (Original) The bonding pad structure as claimed in claim 24, wherein the circuit under pad (CUP) scheme comprises:

a plurality of via holes formed in the first dielectric layer and underlying the extension portion of the first conductive layer,

wherein the conductive plugs are formed in the via holes respectively; and

wherein the circuit scheme is formed in the first dielectric layer and underlying the conductive plugs.

27. (Original) The bonding pad structure as claimed in claim 23, wherein the circuit under pad (CUP) scheme comprises:

a second dielectric layer formed underlying the first dielectric layer;

a third conductive layer formed in the second dielectric layer and electrically connected to the first conductive layer;

an extension portion of the third conductive layer extending away from the bonding region and the sensing region;

a buffer layer formed underlying the second dielectric layer;

a circuit scheme formed in the buffer layer; and

a plurality conductive plugs electrically connecting the circuit scheme to the extension portion of the third conductive layer.

28. (Original) The bonding pad structure as claimed in claim 27, wherein the third conductive layer is a ring, a lattice form, an array of islands or a solid form.

29. (Original) The bonding pad structure as claimed in claim 1, further comprising a bonding element formed overlying the second conductive layer within the bonding region.

30. (Original) The bonding pad structure as claimed in claim 29, wherein the bonding element is a conductive ball or a conductive bump.

31. (Original) The bonding pad structure as claimed in claim 1, further comprising a barrier layer formed between the first conductive layer and the second conductive layer.

32. (Original) The bonding pad structure as claimed in claim 31, wherein the barrier layer is Ti, TiN, W, WN, Ta, TaN or a combination thereof.

33. (Original) The bonding pad structure as claimed in claim 1, wherein the first conductive layer is copper (Cu), aluminum (Al), AlCu alloy, a copper manganese alloy or a copper-containing alloy.

34. (Original) The bonding pad structure as claimed in claim 1, wherein the second conductive layer is aluminum (Al), AlCu alloy or an aluminum-containing alloy.

35. (Original) The bonding pad structure as claimed in claim 1, wherein the first dielectric layer is plasma oxide, HDP oxide, dielectric with high resistance to mechanical stress, low-k dielectrics, fluorinated silicate glass (FSG) or silicon-based dielectrics.

36-69. (Canceled)